AU OPTRONICS CORPORATION

Product Specification

17.0” WXGA+ Color TFT-LCD Module

Model Name: B170PW03 V9
Dell P/N: UM603

Approved by	Prepared by
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NBBU Marketing Division / AU Optronics corporation

Customer	Checked & Approved by
Dell	

Product Specification

17.0” WXGA+ Color TFT-LCD Module
Model Name: B170PW03 V9
Customer: Dell
Dell Part No: UM603

( ) Preliminary Specifications
(V) Final Specifications

Note: This Specification is subject to change without notice.

Contents

Record of Revision

Version and Date	Page	Old description	New Description	Remark
V0 2006/1/2	All	First Edition		

1. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(, IEC60950 or UL1950), or be applied exemption.
14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit(IEC60950 or UL1950). Do not connect the CCFL in Hazardous Voltage Circuit.

2. General Description

B170PW03 V9 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA+ (1440(H) x 900(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter of backlight is not included.

B170PW03 V9 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 General Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

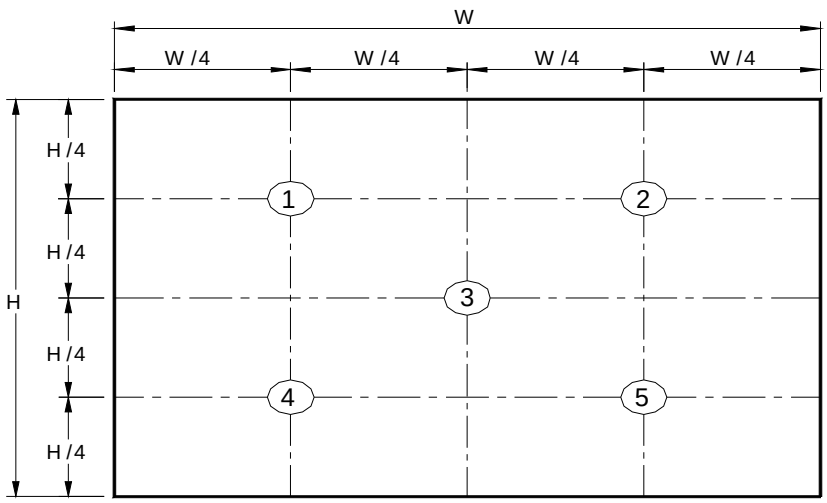
Items	Unit	Specifications
Screen Diagonal	[mm]	17.0”
Active Area	[mm]	367.20(H) x 229.50(V)
Pixels H x V		1440x3(RGB) x 900
Pixel Pitch	[mm]	0..255(per one triad) x 0.255
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance (ICCFL=6.5mA)	[cd/m^2]	220 typ. (5 points average) 200 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		500 typ.
Response time	[msec]	16 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Typical Power Consumption	[Watt]	7.5 W max. (without Inverter)
Weight	[Grams]	700 g max.
Physical Size	[mm]	382.2(W) x 244.5(H) x 6.5(D) typ;. 7.0(D) max
Electrical Interface		2 channel LVDS
Surface Treatment		Glare, Harness 3H
Support Color		Native 262K colors (RGB 6-bit data driver)
Temperature Range Operating Storage (Non-Operating)	 [^{o}C] [^{o}C]	 0 to +50 -40 to +65
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

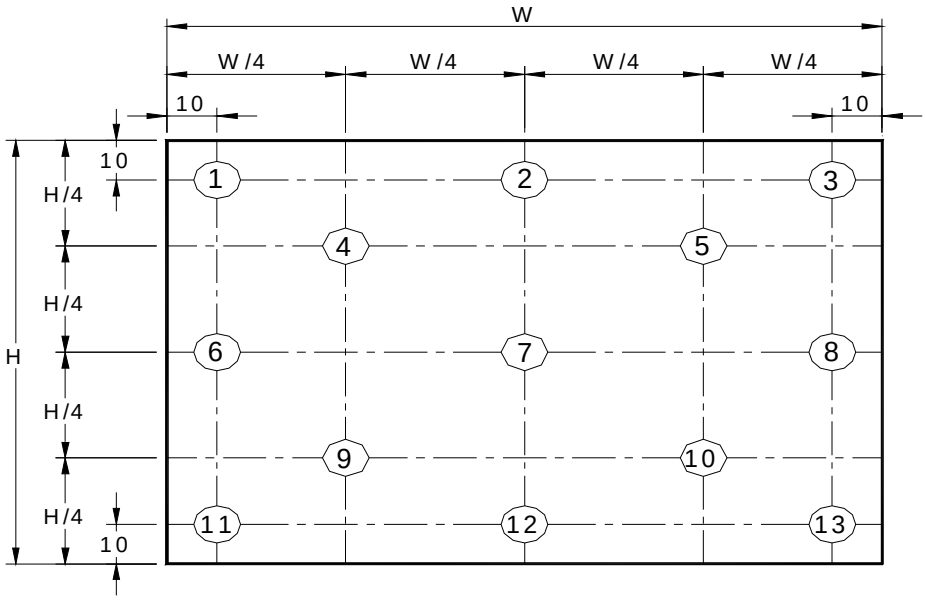
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Luminance CCFL 6.5mA	[cd/m2]	5 points average	200	220	-	1,2,3
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	40 40	45 45	- -	2,7
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	15 30	20 35	- -	
Luminance Uniformity		5 Points			1.25	1
Luminance Uniformity		13 Points			2.0	
CR: Contrast Ratio			400	500	-	6
Cross talk	%				4	4
Response Time	[msec]	Rising	-	12	17	5
	[msec]	Falling	-	4	8	
	[msec]	Raising + Falling		16	25	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.550	0.580	0.610	2,7
		Red y	0.310	0.340	0.370	
		Green x	0.280	0.310	0.340	
		Green y	0.520	0.550	0.580	
		Blue x	0.120	0.150	0.180	
		Blue y	0.090	0.120	0.150	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Display area : 367.20(H) x 229.50(V)mm)



Note 2: 13 points position



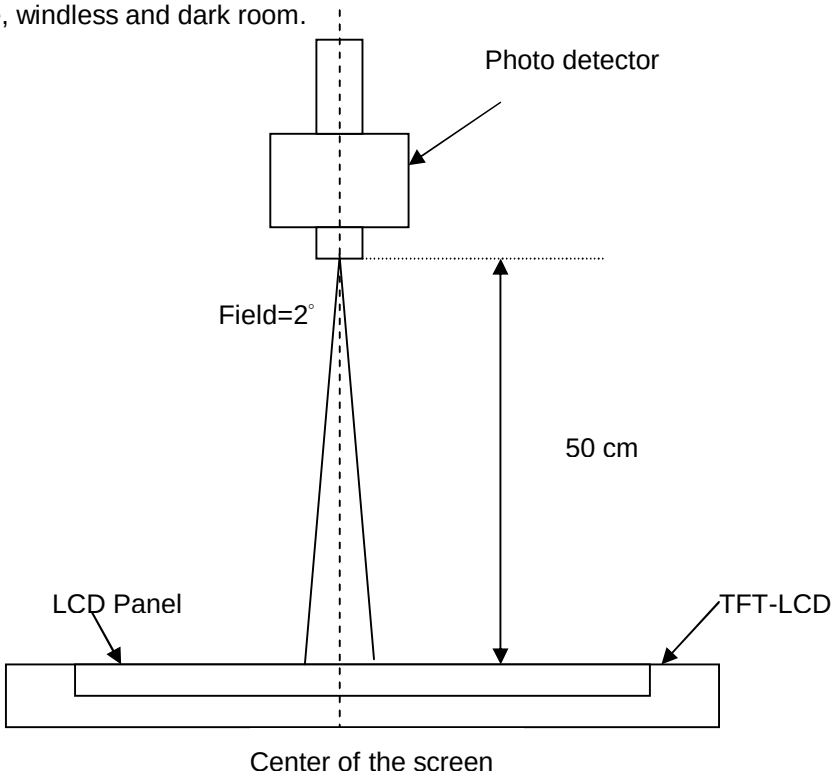
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



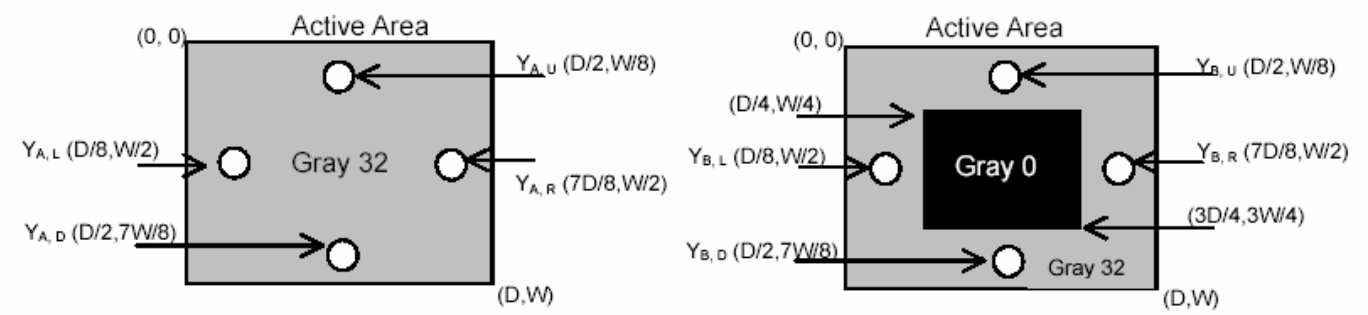
Note 5： Definition of Cross Talk (CT)

CT = | Y_B – Y_A | / Y_A × 100 (%)

Where

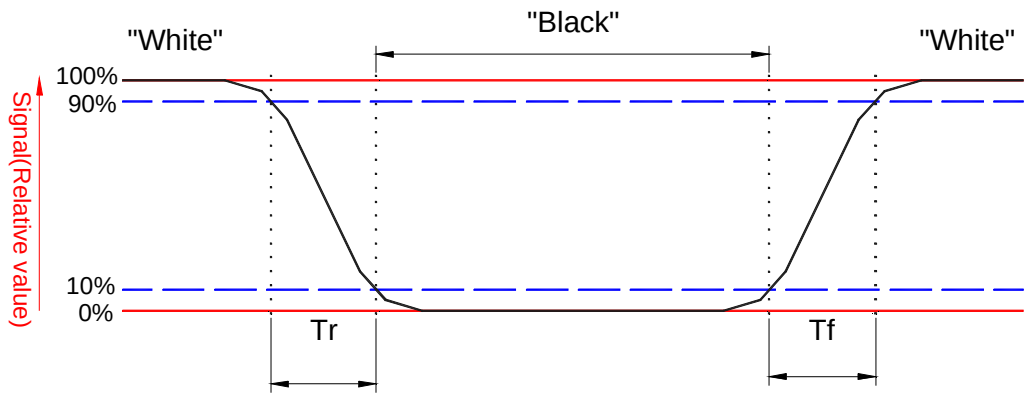
Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



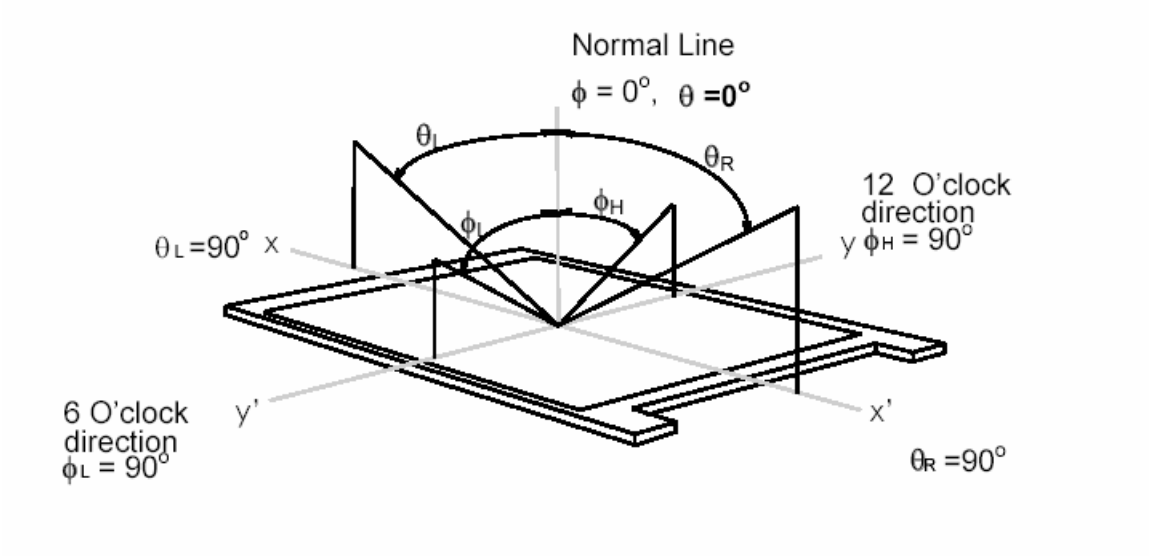
Note 6: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from“Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



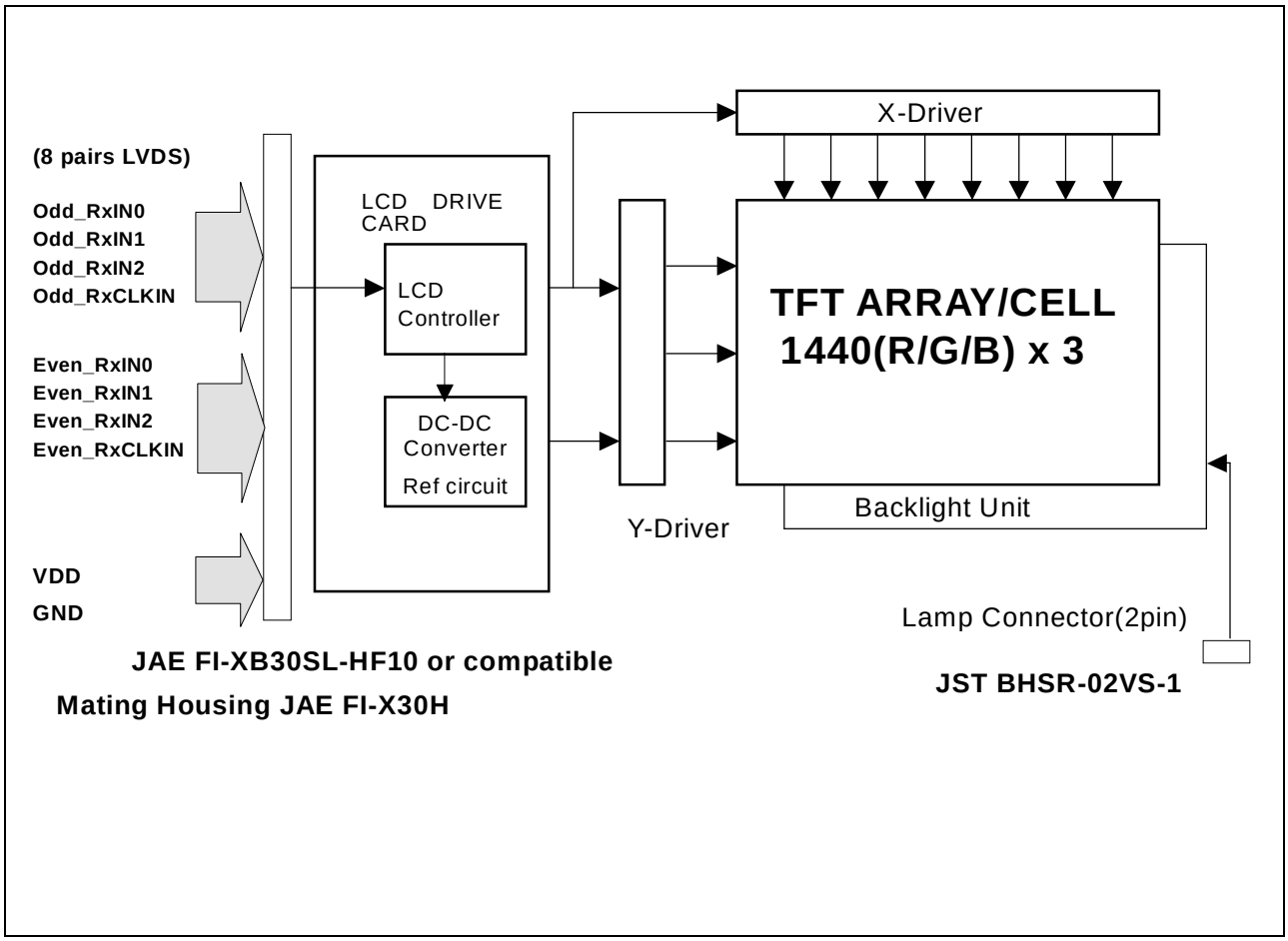
Note 7. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 17.0 inches wide Color TFT/LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICCFL	-	6.5	[mA] rms	Note 1,2

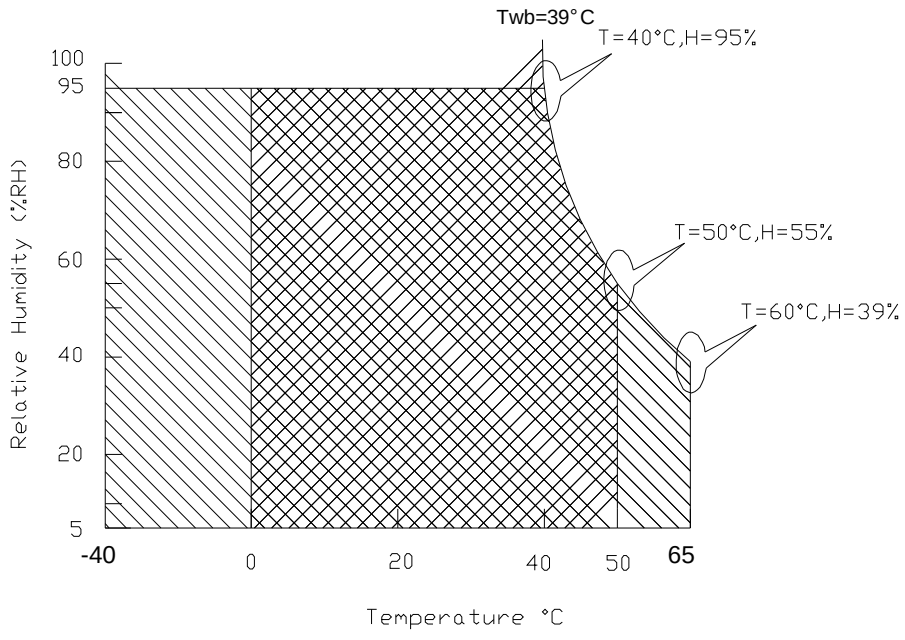
4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[°C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: With in Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality perfermance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range Storage Range

5. Electrical characteristics

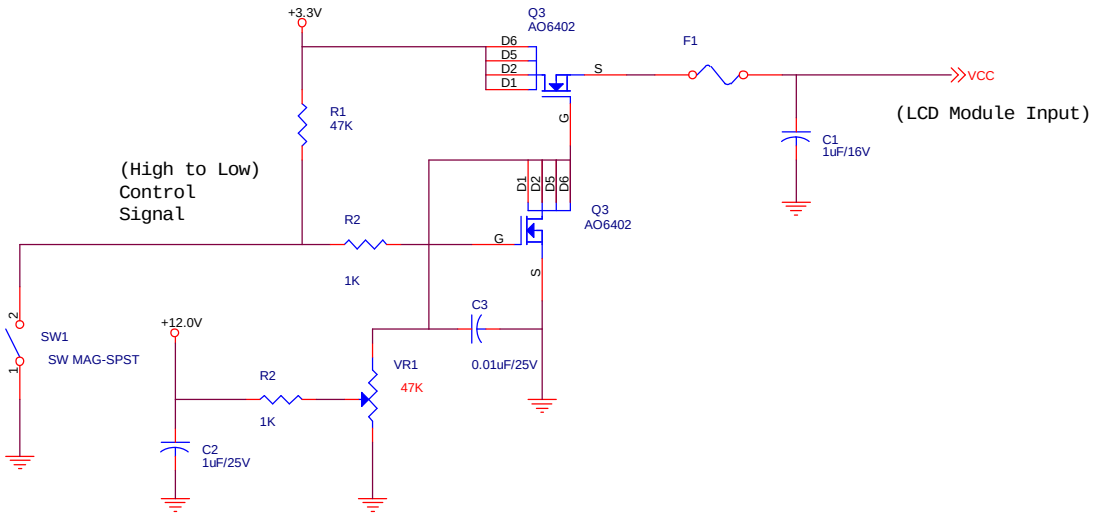
5.1 TFT LCD Module

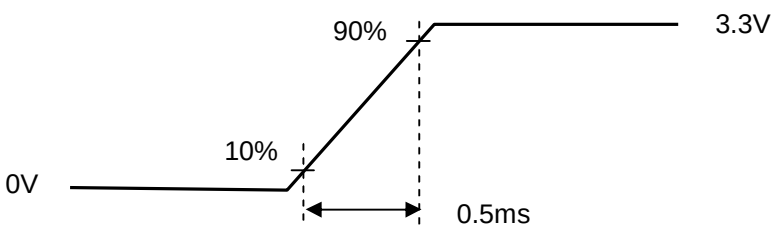
5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		2.15		[Watt	All White pattern
IDD	IDD Current		680		mA	Max:All Black Pattern
IRush	Inrush Current			2000	mA	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	[mV] p-p	

Note 1 : Measurement conditions:





Vin rising

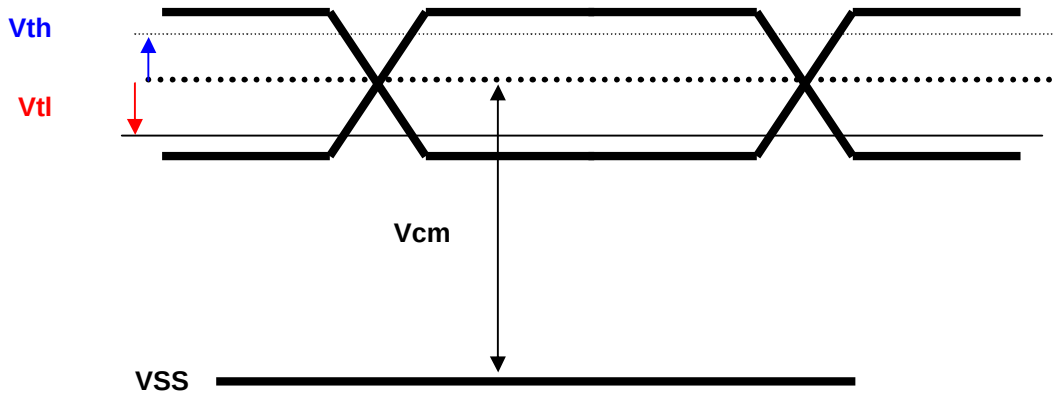
5.1.2 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A(Thine Electronics Inc.) in detail.Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
Vtl	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]
Vcm	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform



5.2 Backlight Unit

Parameter guideline for CCFL Inverter

Parameter	Min	Typ	Max	Units	Condition
White Luminance 5 points average	2800	3100	-	[cd/m^2]	(Ta=25℃)
CCFL current(ICCFL)	3.0	6.5	7.0	[mA] rms	(Ta=25℃) Note 2
CCFL Frequency(FCCFL)	45	50	80	[KHz]	(Ta=25℃) Note 3,4
CCFL Ignition Voltage(Vs)	1500			[Volt] rms	(Ta= 0℃) Note 5
CCFL Voltage (Reference) (VCCFL)	775	815	940	[Volt] rms	(Ta=25℃) Note 6
CCFL Power consumption (PCCFL)		4.9		[Watt]	(Ta=25℃) Note 6

Note 1: Typ are AUO recommended Design Points.

*1 All of characteristics listed are measured under the condition using the AUO Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be employed the inverter which has “Duty Dimming”, if ICFL is less than 4mA.

Note 3: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CFL inverter should be able to give out a power that has a generating capacity of over 1,430 voltage. Lamp units need 1,400 voltage minimum for ignition.

Note 6: Calculator value for reference (ICCFL×VCCFL=PCCFL)

5.3 Inverter Characteristic

5.3.1 Foxconn inverter (with Maxim IC)

Electrical Characteristics : Vin= 7.5V~21V

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input Voltage	INV_SRC	-	7.5	14.0	21.0	V
2	Input Voltage	5VALW	-	4.85	-	5.20	V
3	Input Current	Iin	Vin=14.0V, max. output	-	0.491	-	A
4	Input Power	Pin	Vin=14.0V, Iout=6.5mA	5.76	6.88	7.92	W
5	SMBus Mode Brightness Adjust	SMB_DAT	Min. output: 00H Max. output: FFH	00	-	FF	Hex.
6	DPST mode (System side PWM input)	PWM(Hz)	-	-	10	-	KHz
		PWM Voltage	-	3.0	3.30	5.5	V
		Signal intensity	-	00	-	FF	Hex
7	Output Voltage	Vout	Max. output	-	750	-	Vrms
8	Output Current	Iout (Min)	Ta=25℃, after running 30 min.	1.45	1.75	2.05	mArms
		Iout (Max)		6.3	6.5	6.8	mArms
9	Frequency	Freq	Max. output	45	55	65	KHz
10	Output Power	Pout	Vin=14.0V, Iout(Max)	4.17	4.88	5.61	W
11	Burst Mode Frequency	f_B		200	210	220	Hz
12	Ambient Light input signal			5	-	1000	Lux
13	Open Lamp Voltage(2)	Vopen	No Load	1500	-	-	Vrms
14	Striking Time	Ts	No Load	0.6	1.0	1.4	Sec
15	Efficiency	η	Vin=7.5V, Max. output, Load=100K	-	80	-	%
16	Start –up time			-	-	0.1	Sec

5.3.2 Sumida inverter (with MPS IC)

Electrical Characteristics : Vin= 7.5V~21V

	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input Voltage	Vin		7.5	14.4	21	V
2	Input Current	Iin	Vin=7.5V,SMB_DATA=FFH,PWM DUTY =100%,AMBIENT LIGHT=1000LUX	730	790	850	mA
3	Input Power	Pin	Vin=21V,SMB_DATA=FFH,PWM DUTY =100%,AMBIENT LIGHT=1000LUX	---	6.3	---	W
4	Input Signal Level for 5VSUS,5VALW			4.85	5	5.2	V
5	Backlight Adjust(Lamp current control)		SMB_DATA=FFH,PWM DUTY =100%,AMBIENT LIGHT=1000LUX	00H	--	FFH	
6	Output Voltage	Vout	SMData=FFH	630	700	770	Vrms
7	Output current	Iout(Min)	Vin(7.5~21V)SMB_DATA=00H,PWM DUTY =100%,AMBIENT LIGHT=1000LUX Ta=25℃,after running 30 min	1.25	1.55	1.85	mArms mArms
		Iout(Max)	Vin(7.5~21V)SMB_DATA=FFH,PWM DUTY =100%,AMBIENT LIGHT=1000LUX Ta=25℃,after running 30 min	6.2	6.5	6.8	mArms
8	Frequency	Freq	Vin=7.5~21V	45	55	65	KHz
9	Output power	Pout	Vin=21V SMB_DATA=FFH,PWM DUTY =100%,AMBIENT LIGHT=1000LUX	---	4.55	---	W
10	Open lamp voltage	Vopen	No load	1400	--	1800	Vrms
11	Striking time	Ts	Vin=7.5~21V	0.6	1	1.4	Sec
12	Efficiency	η	Vin=7.5V,Iout=Max. Load=115KΩ//15PF TO GND	80	--	--	%

5.3.2 Sumida inverter (with MPS IC)

Electrical Characteristics : Vin= 7.5V~21V

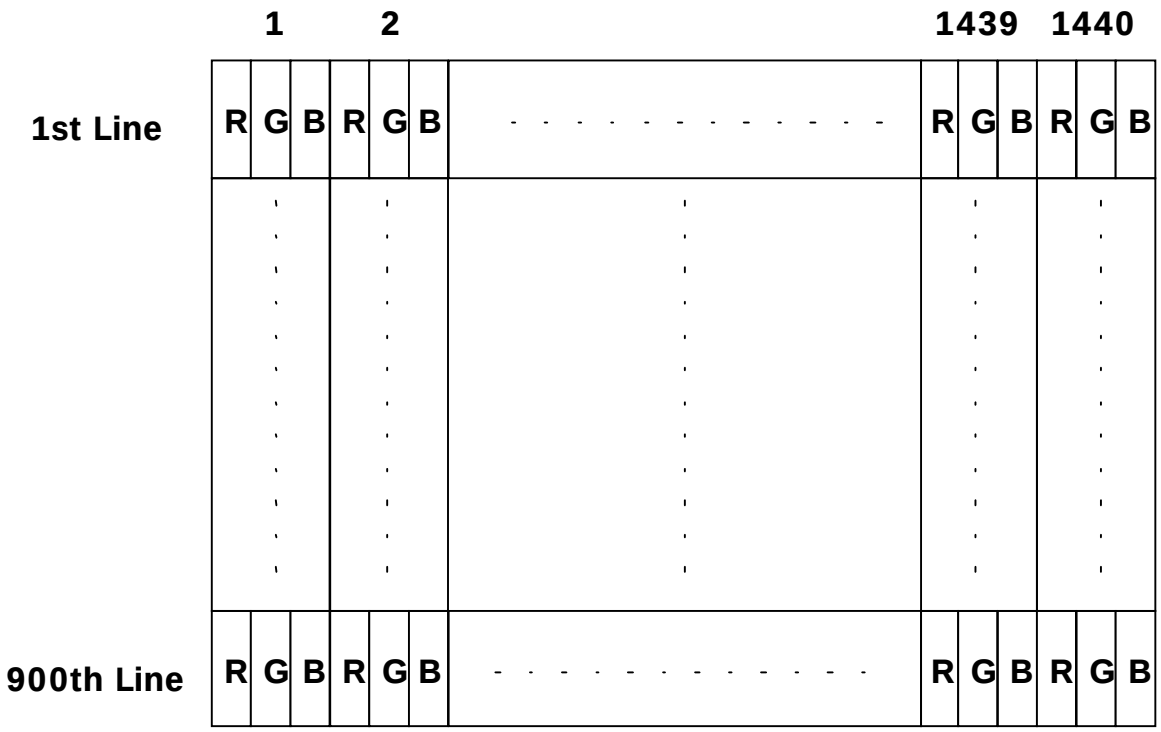
Electrical Characteristics Ta=25℃ (P/N : T73I017.00 Rev. : 0)

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Input Voltage	INV_SRC	-	7.5	14.0	21.0	V
2	Input Voltage	5VALW	-	4.75	-	5.20	V
3	Input Current	Iin	Vin=14.0V, max. output	0.411	0.491	0.565	A
4	Input Power	Pin	Vin=14.0V, Iout=6.5mA	5.75	6.88	7.91	W
5	SMBus Mode Brightness Adjust	SMB_DAT	Min. output: 00H Max. output: FFH	00	-	FF	Hex.
6	DPST mode (System side PWM input)	PWM(Hz)	-	-	10	-	KHz
		PWM Voltage	-	3.135	3.30	3.465	V
		Signal intensity	-	00	-	FF	Hex
7	Output Voltage	Vout	Max. output	650	750	850	Vrms
8	Output Current	Iout (Min)	Ta=25℃, after running 30 min.	1.25	1.55	1.85	mArms
		Iout (Max)		6.20	6.50	6.80	mArms
9	Frequency	Freq	Max. output	45	55	65	KHz
10	Output Power	Pout	Vin=14.0V, Iout(Max)	4.17	4.88	5.61	W
11	Burst Mode Frequency	f_B		200	210	220	Hz
12	Ambient Light input signal			3	-	320	Lux
13	Open Lamp Voltage(2)	Vopen	No Load	1400	-	1800	Vrms
14	Striking Time	Ts	No Load	0.6	1.0	1.4	Sec
15	Efficiency	η	Vin=7.5V, Max. output, Load=100K	-	80	-	%
16	Start –up time			-	-	0.1	Sec

6. Signal Characteristic

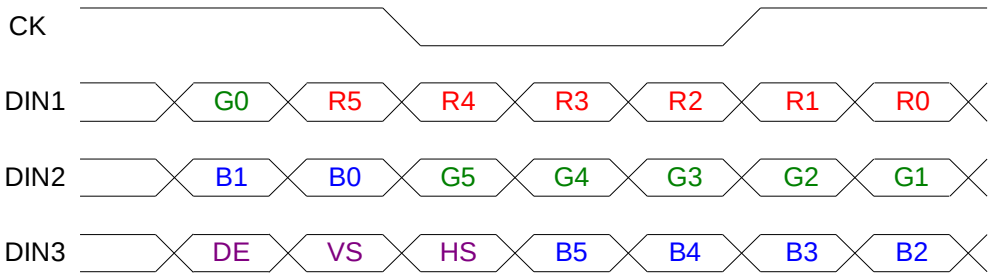
6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

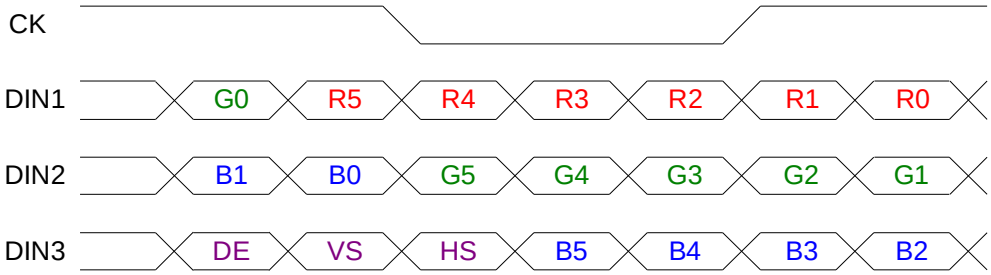


6.2 The input data format

ODD pair(1st pixel input)



Even pair(2nd pixel input)



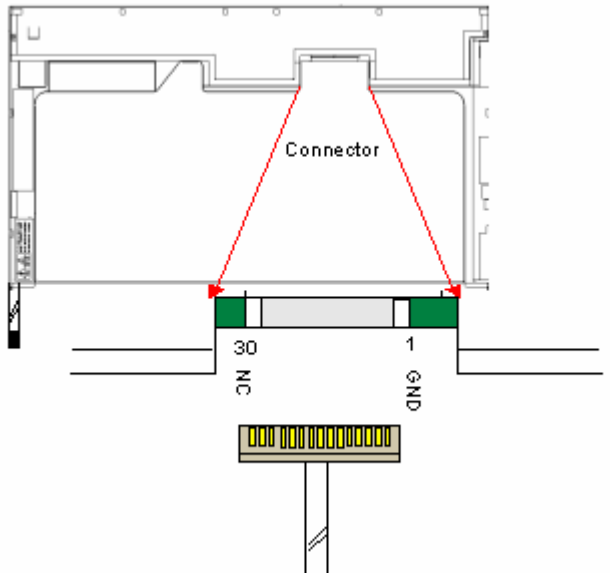
Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) **Red-pixel Data**	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) **Green-pixel Data**	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) **Blue-pixel Data**	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	**Data Clock**	The typical frequency is 48.2 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DE	**Display Timing**	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VS	**Vertical Sync**	The signal is synchronized to -DTCLK .
HS	**Horizontal Sync**	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

6.3 Signal Description

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

Pin no	Symbol	Function	Etc.
1	GND	Ground	
2	VDD	Power supply ,3.3 V (typical)	
3	VDD	Power supply ,3.3 V (typical)	
4	V_{EDID}	DDC 3.3V power	
5	NC	No Connection (Reserved for AUO) test	
6	CLK_{EDID}	DDC Clock	
7	$Data_{EDID}$	DDC data	
8	Odd_RxIN0-	-LVDS differential data input	
9	Odd_RxIN0+	+LVDS differential data input	
10	GND	Ground	
11	Odd_RxIN1-	-LVDS differential data input	
12	Odd_RxIN1+	+LVDS differential data input	
13	GND	Ground	
14	Odd_RxIN2-	-LVDS differential data input	
15	Odd_RxIN2+	+LVDS differential data input	
16	GND	Ground	
17	Odd_RxCLKIN-	-LVDS differential clock input	
18	Odd_RxCLKIN+	+LVDS differential clock input	
19	GND	Ground	
20	Even_RxIN0-	-LVDS differential data input	
21	Even_RxIN0+	+LVDS differential data input	
22	GND	Ground	
23	Even_RxIN1-	-LVDS differential data input	
24	Even_RxIN1+	+LVDS differential data input	
25	GND	Ground	
26	Even_RxIN2-	-LVDS differential data input	
27	Even_RxIN2+	+LVDS differential data input	
28	GND	Ground	
29	Even_RxCLKIN-	-LVDS differential clock input	
30	Even_RxCLKIN+	+LVDS differential clock input	



Note1: Start from right side

Note2: Please follow VESA standard.
Note3: Input signals shall be low or High-impedance when VDD is off.
Internal circuit of LVDS inputs are as following.
The module uses a 100ohm resistor between positive and negative data lines of each receiver input

6.4 Interface Timing

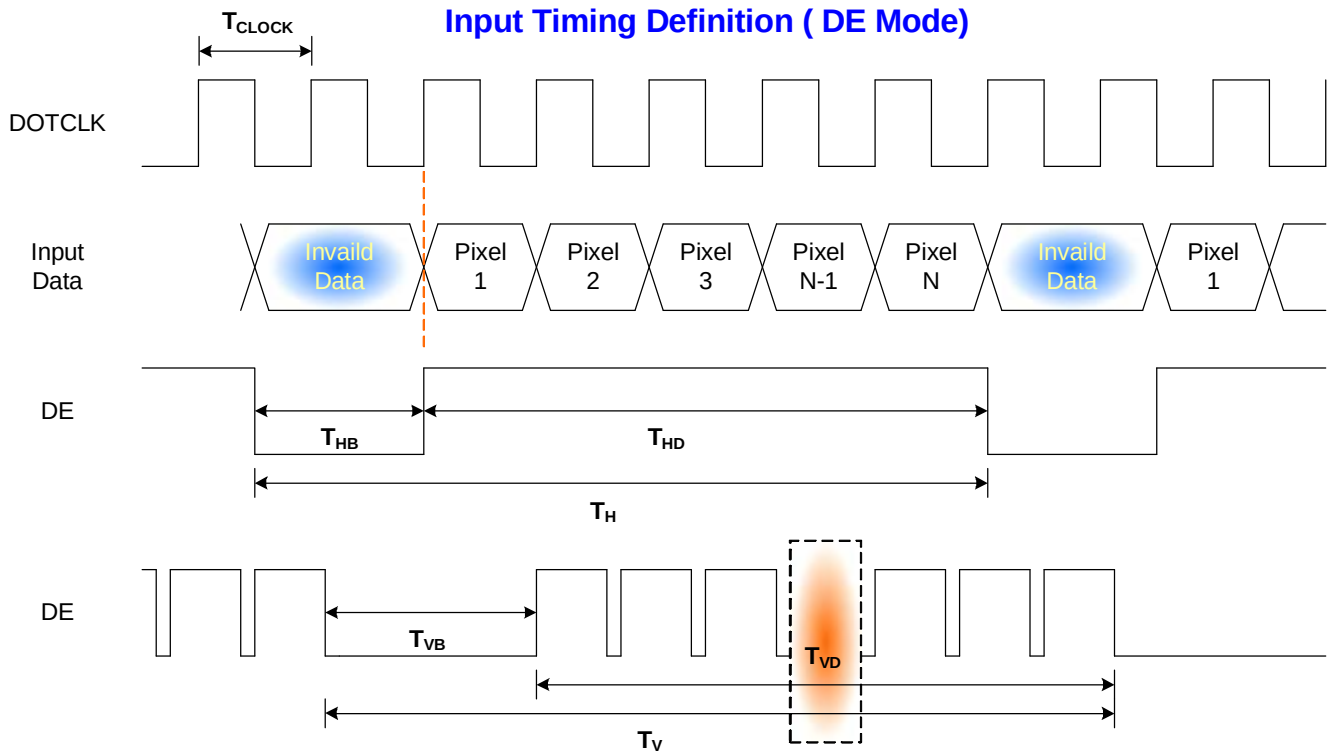
6.4.1 Timing Characteristics

Basically, interface timings should match the 1440x900 manufacturing guide line timing.

Signal	Item	Symbol	Min	Typ	Max	Unit
Vertical Section	Period	Tv	904	912	2048	Th
	Active	Tdisp(v)	900	900	900	Th
	Blanking	Tblk(v)	4	12	-	Th
Horizontal Section	Period	Th	760	880	1024	Tclk
	Active	Tdisp(h)	720	720	720	Tclk
	Blanking	Tblk(h)	40	160	-	Tclk
Clock	Period	Tclk	16.61	20.75	-	ns
	Frequency	Freq	-	48.2	60.2	MHz

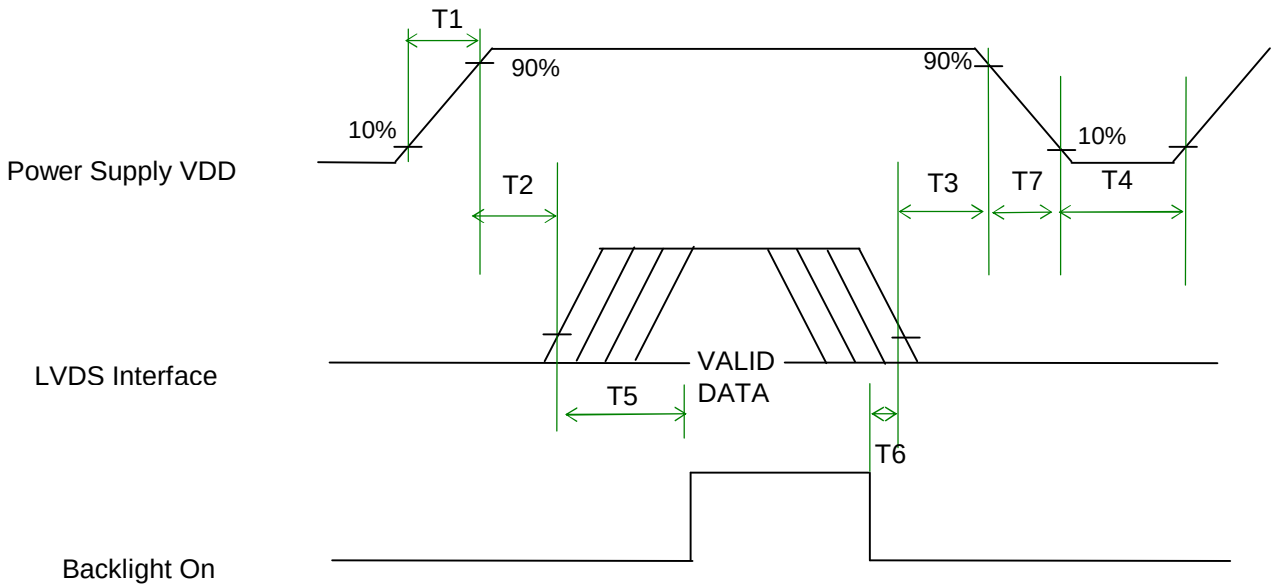
Note : DE mode only

6.4.2 Timing diagram



6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



Power Sequence Timing

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	400	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

Connector Name / Designation	For Signal Connector
Manufacturer	JAE or compatible
Type / Part Number	FI-XB30SL-HF10 or compatible
Mating Housing/Part Number	FI-X30H
Mating Contact/Part Number	FI-XC3-1-15000

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1-TB

7.3 Signal for Lamp connector

Pin #	Cable color	Signal Name
1	Red	Lamp High Voltage
2	White	Lamp Low Voltage

8. Vibration and Shock Test

8.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

- Test method: Non-Operation
- Acceleration: 180 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

9. Reliability

Items	Required Conditions
Operating Life – High Temp.	Temp.= +50°C, Dynamic. 250 Hours, Humidity 20%
Operating Life – Low Temp.	Temp.= 0°C, Dynamic, 250 Hours, Humidity 20%
High Temp. Storage Life – Non-Operating	Temp.= +65°C, Non-Operating, 250 Hours, Humidity 20%
Low Temp. Storage Life – Non-Operating	Temp.= -40°C, Non-Operating, 250 Hours
High Temp & High Humidity Operating Life	Temp.=+40°C,Dynamic,Humidity 95%(Non-Condensing), 250 Hours
Shock – Non-Operating	180g, 2.0 ms, Half Sine Wave
Vibration – Non-Operating	Random vibration, 1.5 G zero-to-peak, 10 to 500 Hz, 30 mins in each of three mutually perpendicular axes
Temp. Cycle – Operating	0℃ to +40℃ ,Ramp< 20℃ /min, Duration at Temp. = 30 min, Test Cycles =160
Temp. Cycle – Non-Operating	-40°C to +65°C, Ramp ≤20°C/min, Duration at Temp. = 30min, Test Cycles = 50
ESD	Contact : ±8KV/ operation Air : ±15KV / operation
Room temperature Test	25℃, 2000hours, Operating with loop pattern

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

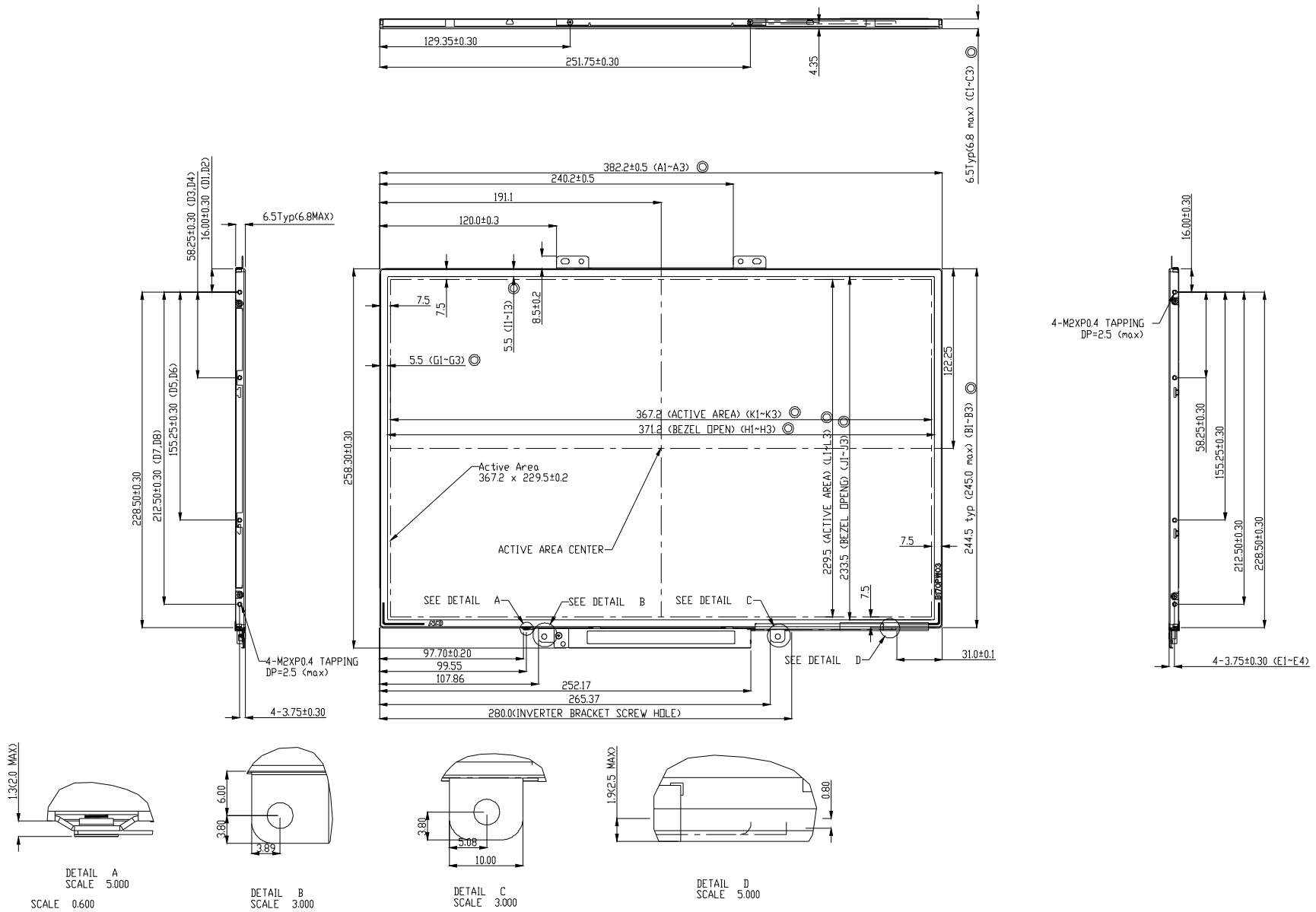
. Self-recoverable. No hardware failures.

Note2: CCFL Life time: 10,000 hours minimum under normal module usage.

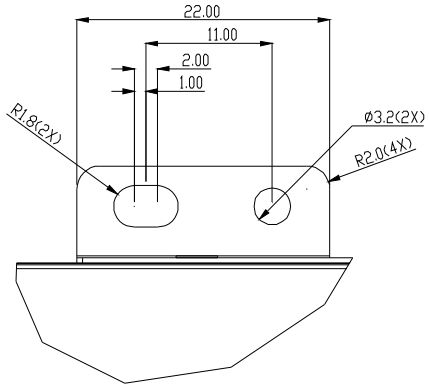
Note3: MTBF (Excluding the CCFL): 30,000 hours with a confidence level 90%

10. Mechanical Characteristics

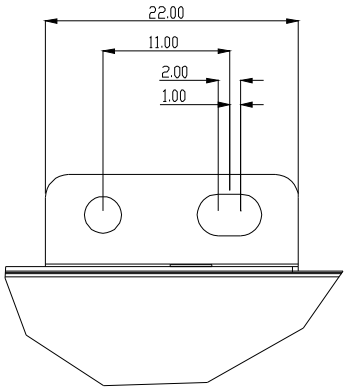
10.1 LCM Outline Dimension(Front View)



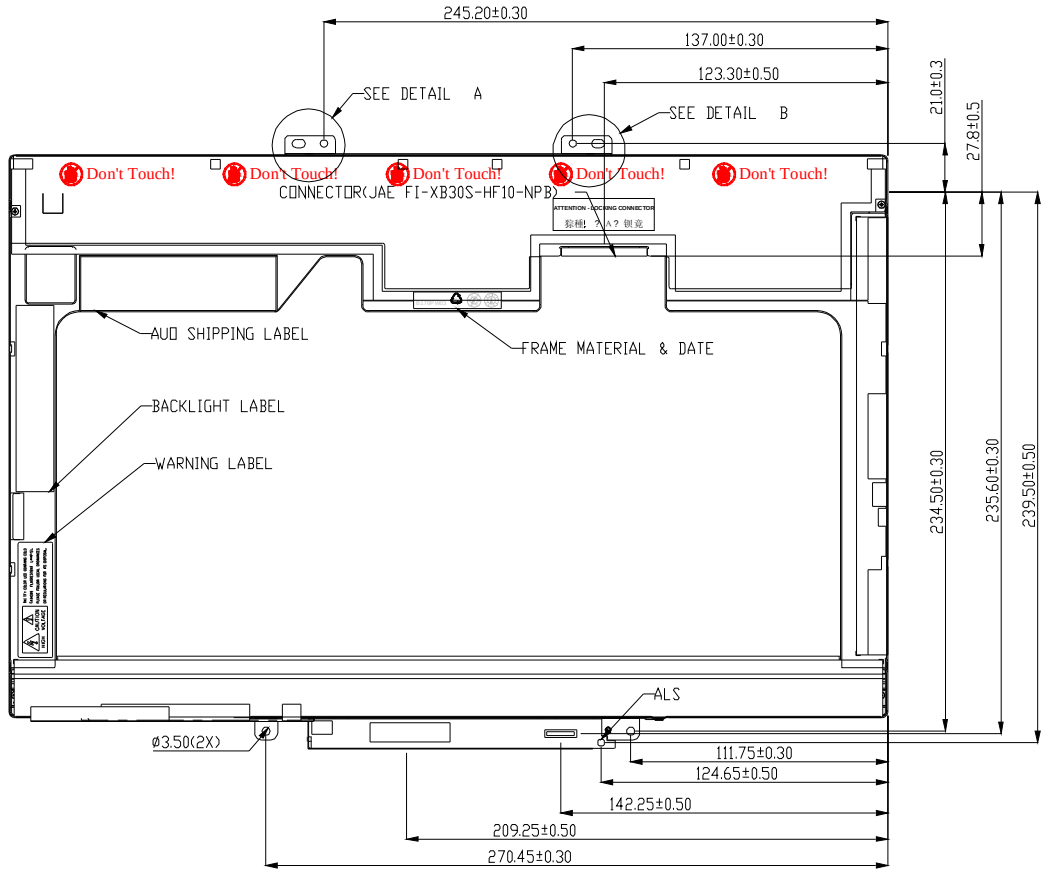
10.2 LCM Outline Dimension(Rear View)



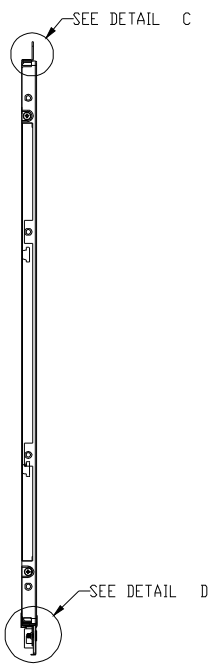
DETAIL A
SCALE 3.000

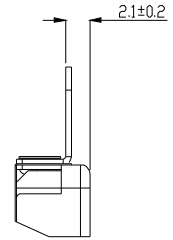


DETAIL B
SCALE 3.000

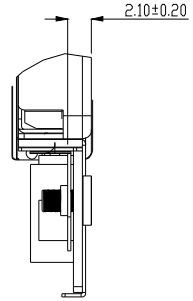


SCALE 0.600





DETAIL C
SCALE 3.000



DETAIL D
SCALE 3.000

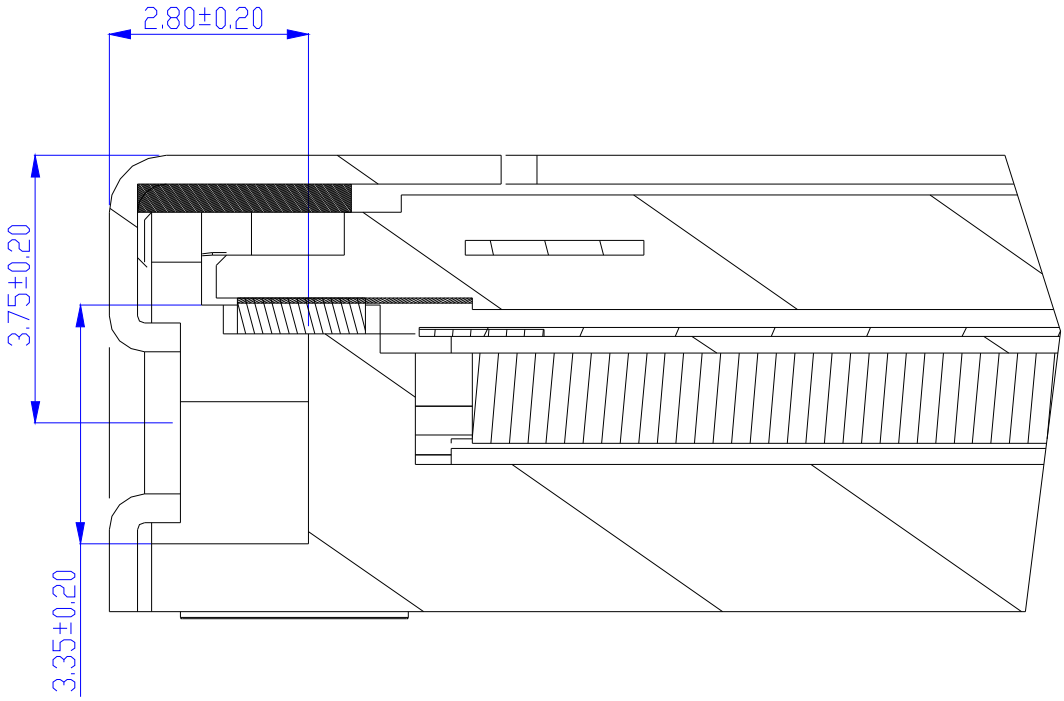
10.3 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface =2.6 mm (See drawing)

Screw hole center location, from front surface = 3.75 ± 0.2mm (See drawing)

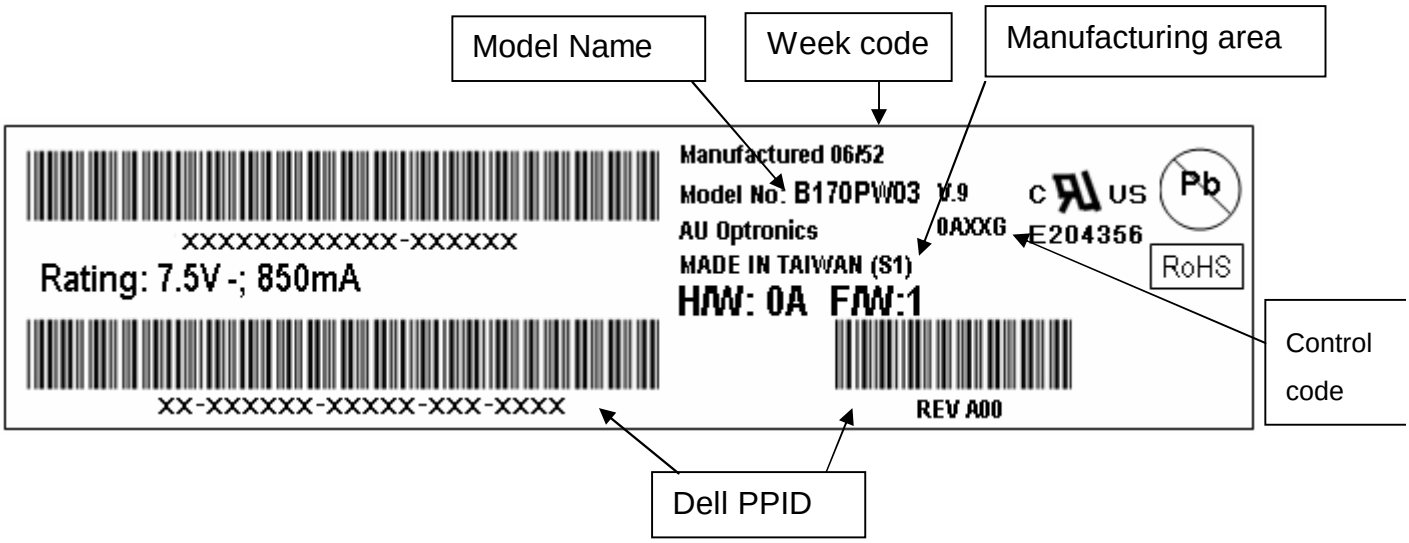
Screw maximum length = 2.3 mm (See drawing)

Screw Torque: Maximum2.5 kgzf-cm

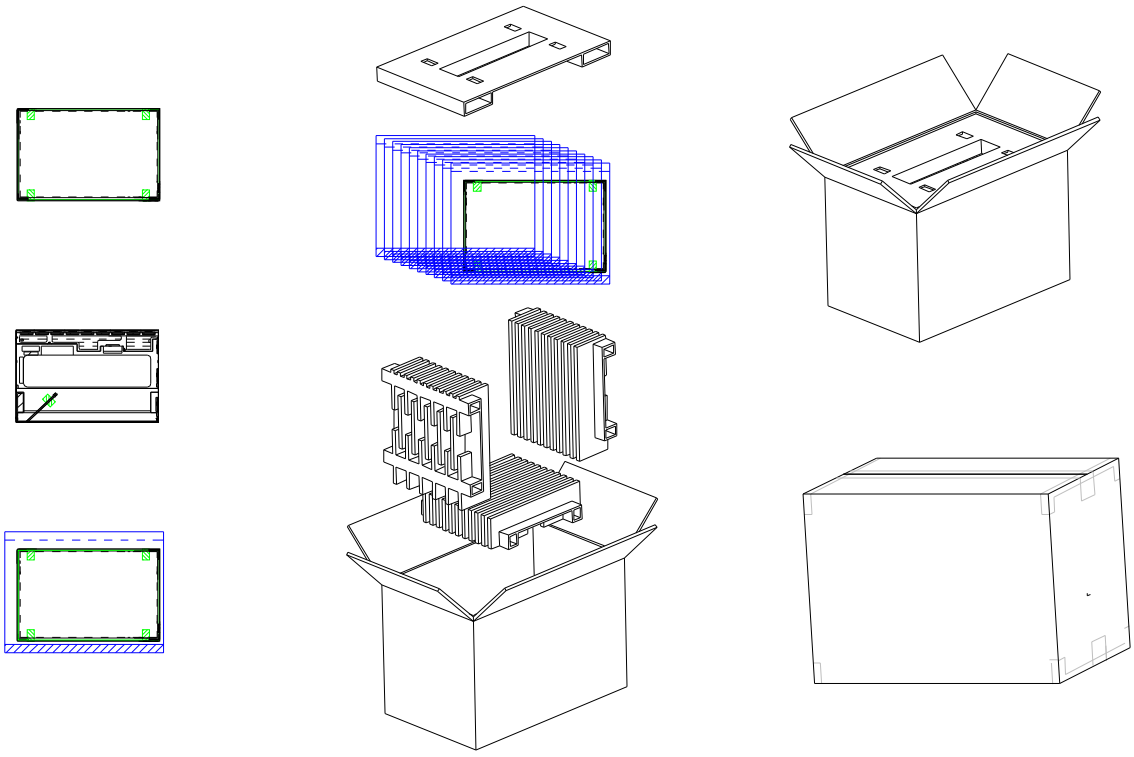


11. Shipping and Package

11.1 Shipping Label Format



11.2. Carton package



12. Appendix: EDID description

Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)	Value (DEC)
0	Header	00	00000000	0
1	Header	FF	11111111	255
2	Header	FF	11111111	255
3	Header	FF	11111111	255
4	Header	FF	11111111	255
5	Header	FF	11111111	255
6	Header	FF	11111111	255
7	Header	00	00000000	0
8	EISA manufacture code = 3 Character ID	06	00000110	6
9	EISA manufacture code (Compressed ASCII)	AF	10101111	175
0A	Panel Supplier Reserved – Product Code	87	10000111	135
0B	Panel Supplier Reserved – Product Code	39	00111001	57
0C	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0D	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0E	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
0F	LCD module Serial No - Preferred but Optional (“0” if not used)	00	00000000	0
10	Week of manufacture	01	00000001	1
11	Year of manufacture	11	00010001	17
12	EDID structure version # = 1	01	00000001	1
13	EDID revision # = 3	03	00000011	3
14	Video I/P definition = Digital I/P (80h)	80	10000000	128
15	Max H image size = (Rounded to cm)	25	00100101	37
16	Max V image size = (Rounded to cm)	17	00010111	23
17	Display gamma = (gamma ×100)-100 = Example: (2.2×100) – 100 = 120	78	01111000	120
18	Feature support (no DPMS, Active off, RGB, timing BLK 1)	0A	00001010	10
19	Red/Green Low bit (RxRy/GxGy)	87	10000111	135
1A	Blue/White Low bit (BxBy/WxWy)	B5	10110101	181
1B	Red X Rx = 0.580	94	10010100	148
1C	Red Y Ry = 0.340	57	01010111	87
1D	Green X Gx = 0.310	4F	01001111	79
1E	Green Y Gy = 0.550	8C	10001100	140
1F	Blue X Bx = 0.150	26	00100110	38
20	Blue Y By = 0.120	1E	00011110	30
21	White X Wx = 0.313	50	01010000	80
22	White Y Wy = 0.329	54	01010100	84
23	Established timings 1 (00h if not used)	00	00000000	0
24	Established timings 2 (00h if not used)	00	00000000	0

25	Manufacturer's timings (00h if not used)	00	00000000	0
26	Standard timing ID1 (01h if not used)	01	00000001	1
27	Standard timing ID1 (01h if not used)	01	00000001	1
28	Standard timing ID2 (01h if not used)	01	00000001	1
29	Standard timing ID2 (01h if not used)	01	00000001	1
2A	Standard timing ID3 (01h if not used)	01	00000001	1
2B	Standard timing ID3 (01h if not used)	01	00000001	1
2C	Standard timing ID4 (01h if not used)	01	00000001	1
2D	Standard timing ID4 (01h if not used)	01	00000001	1
2E	Standard timing ID5 (01h if not used)	01	00000001	1
2F	Standard timing ID5 (01h if not used)	01	00000001	1
30	Standard timing ID6 (01h if not used)	01	00000001	1
31	Standard timing ID6 (01h if not used)	01	00000001	1
32	Standard timing ID7 (01h if not used)	01	00000001	1
33	Standard timing ID7 (01h if not used)	01	00000001	1
34	Standard timing ID8 (01h if not used)	01	00000001	1
35	Standard timing ID8 (01h if not used)	01	00000001	1
36	Pixel Clock/10,000 (LSB)	9E	10011110	158
37	Pixel Clock/10,000 (MSB)	25	00100101	37
38	Horizontal Active = 1024 pixels (lower 8 bits)	A0	10100000	160
39	Horizontal Blanking (Thbp) = 320 pixels (lower 8 bits)	40	01000000	64
3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	51	01010001	81
3B	Vertical Active = 768 lines	84	10000100	132
3C	Vertical Blanking (Tvbp) = 38 lines (DE Blanking typ. for DE only panels)	0C	00001100	12
3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48
3E	Horizontal Sync, Offset (Thfp) = 26 pixels	40	01000000	64
3F	Horizontal Sync, Pulse Width = 136 pixels	20	00100000	32
40	Vertical Sync, Offset (Tvfp) = 3 lines Sync Width = 6 lines	33	00110011	51
41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
42	Horizontal Image Size =304 mm	6F	01101111	111
43	Vertical image Size = 228 mm	E6	11100110	230
44	Horizontal Image Size / Vertical image size	10	00010000	16
45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives, DE only note: LSB is set to "1" if panel is DE-timing only. H/V can be ignored.	19	00011001	25

48	Pixel Clock/10,000 (LSB)	5A	01011010	90
49	Pixel Clock/10,000 (MSB)	1F	00011111	31
4A	Horizontal Active = xxxx pixels (lower 8 bits)	A0	10100000	160
4B	Horizontal Blanking (Thbp) = xxxx pixels(lower 8 bits)	40	01000000	64
4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	51	01010001	81
4D	Vertical Active = xxxx lines	84	10000100	132
4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	0C	00001100	12
4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000	48
50	Horizontal Sync, Offset (Thfp) = xxxx pixels	40	01000000	64
51	Horizontal Sync, Pulse Width = xxxx pixels	20	00100000	32
52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	33	00110011	51
53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
54	Horizontal Image Size =xxx mm	6F	01101111	111
55	Vertical image Size = xxx mm	E6	11100110	230
56	Horizontal Image Size / Vertical image size	10	00010000	16
57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000	0
58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000	0
59	Module “A” Revision = Example: 00, 01, 02, 03, etc.	00	00000000	0
5A	Flag	00	00000000	0
5B	Flag	00	00000000	0
5C	Flag	00	00000000	0
5D	Dummy Descriptor	FE	11111110	254
5E	Flag	00	00000000	0
5F	Dell P/N 1st Character	55	01010101	85
60	Dell P/N 2nd Character	4D	01001101	77
61	Dell P/N 3rd Character	36	00110110	54
62	Dell P/N 4th Character	30	00110000	48
63	Dell P/N 5th Character	33	00110011	51
64	LCD Supplier EEDID Revision #	00	00000000	0
65	Manufacturer P/N	42	01000010	66
66	Manufacturer P/N	31	00110001	49
67	Manufacturer P/N	37	00110111	55
68	Manufacturer P/N	30	00110000	48
69	Manufacturer P/N	50	01010000	80
6A	Manufacturer P/N	57	01010111	87
6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	33	00110011	51
6C	Flag	00	00000000	0
6D	Flag	00	00000000	0

6E	Flag	00	00000000	0
6F	Data Type Tag:	FE	11111110	254
70	Flag	00	00000000	0
71	SMBUS Value = 10 nits	2B	00101011	43
72	SMBUS Value = 17 nits	3D	00111101	61
73	SMBUS Value = 24 nits	4A	01001010	74
74	SMBUS Value = 30 nits	54	01010100	84
75	SMBUS Value = 60 nits	76	01110110	118
76	SMBUS Value = 100 nits	97	10010111	151
77	SMBUS Value = 160 nits	C7	11000111	199
78	SMBUS Value = max nits (Typically = 00h, XXX nits)	FF	11111111	255
79	Number of LVDS receiver chips = ‘01’ or ‘02’	02	00000010	2
7A	BIST Enable: Yes = ‘01’ No = ‘00’	01	00000001	1
7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010	10
7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000	32
7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000	0
7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	0B	00001011	11